module shifting(clk,a,w);

input clk;

input [7:0]a;

output reg [7:0]w;

reg [7:0]i;

always@(posedge clk)

begin

for(i=8'b0;i<a;i=i+1)

begin

if(a==1<<i)

w<=i;

end

end

endmodule